Abstracts

Simple and accurate technique for extracting the parasitic resistances of the dual-gate GaAs MESFET

M. Ibrahim, B. Syrett and J. Bennett. "Simple and accurate technique for extracting the parasitic resistances of the dual-gate GaAs MESFET." 2002 Microwave and Wireless Components Letters 12.8 (Aug. 2002 [MWCL]): 284-286.

A procedure to extract the extrinsic resistances of the dual-gate GaAs MESFET (DGFET) is described. Six dc measurement setups are used to generate nine independent relations from which all the unknown extrinsic resistances of the DGFET are extracted. The described technique distinguishes between the forward bias and the nonforward bias values of the channel resistance. The extrinsic resistances of 29 devices with different topologies are determined using the developed technique. The extracted resistances follow normal scaling rules versus gate width. The developed procedure is a practical and accurate approach to extract the extrinsic resistances of the DGFET.

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